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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

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EXAMINER	
VERBRUGGE, KEVIN	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 08/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,361	WOO ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35,38-40,52 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35,38-40,52 and 53* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This second non-final Office action is in response to Amendment A, paper #6, filed 7/8/03 by fax which canceled claims 36, 37, and 41-51. Contrary to Applicant's assertion in the first paragraph of the amendment that claims 1-53 are pending, only claims 1-35, 38-40, 52, and 53 are pending due to the cancellation of the above claims. All objections and rejections not repeated below are withdrawn.

Claim Objections

Claim 20 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim or amend the claim to place the claim in proper dependent form.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-8, 10, 11, 12, 14-18, 25-26, 28, 29, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 1, 4, 5, 11, 14, 15, 16, 25, and 26, Ohsawa discloses the claimed plurality of dynamically refreshable memory cells as the DRAM cell array in Fig. 5.

He shows the claimed dynamically changeable use registers corresponding to groups of memory cells as refresh flags, shown in Figs. 4 and 5.

His memory device is configured to omit refreshing of memory cells that are not in use, as claimed, as indicated by the refresh flags.

Regarding claims 2 and 12, in section 4.3, last paragraph, Ohsawa mentions static mode which is the claimed self-refresh mode.

Regarding claims 6, 17, and 28, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claim 7, Ohsawa's row of memory cells is a set of memory cells.

Regarding claims 8, 18, and 29, Ohsawa's refresh flags refer to rows as claimed.

Regarding claim 10, a page of memory cells is the same as a row of memory cells.

Regarding claim 31, Ohsawa shows his use registers in the memory devices in Figs. 4, 5, 7, and 8.

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Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 8, 10-16, 18-20, 23-27, 29, 31-33, 35, 38-39, 52, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer.

Boyer discloses a method and apparatus for leveraging history bits to optimize memory refresh performance.

Boyer discloses or suggests all of the claimed features throughout his disclosure. Particularly relevant portions of his disclosure include Figs. 2, 3, 8, 9, and 16 and

passages at column 2, lines 49-60, column 3, lines 22-27, column 4, lines 14-21 and 60-64, column 5, lines 17-20, column 7, lines 12-18 and 46-51, column 8, lines 1-3 and 26-30, column 10, lines 62-67, column 14, lines 16-19 and 31-34, column 23, lines 2-7, and column 25, line 50 through column 26, line 25.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 9, 17, 21, 22, 28, 30, 34, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer in view of "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 6, 17, 21, 28, 34, and 40, Boyer does not mention caching in his disclosure.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include caching in Boyer's device to speed up system operation and it would have been obvious to one of ordinary skill in the art at the time the

invention was made to include Ohsawa's technique of not refreshing those rows that were cached to further speed up system operations by not having to refresh those rows that were cached, as taught by Ohsawa.

Regarding claim 9, Boyer's refresh flags refer to rows. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use refresh flags for a bank since this would allow an entire bank to be shutdown if its refresh flag were not set, avoiding the need to read the refresh flag of each row.

Regarding claims 22 and 30, Boyer shows that his use registers are outside the DRAM controller (Fig. 8, for example). However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to move the use registers to the memory controller to have more centralized control over the memory cells. Putting the use registers in the memory controller would speed up access to them.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 9, 13, 19, 21-24, 27, 30, 32-35, 38-40, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa in view of U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer.

Regarding claims 3, 13, 19, 27, 32, 33, 35, 38, 39, 52, and 53, Ohsawa does not disclose the claimed recent access flags or keeping track of which memory cells have been accessed in a manner that refreshed the memory cells in a previous memory cycle.

Boyer discloses the recent access flags and keeping track of which memory cells have been accessed in a manner that refreshed the memory cells in a previous memory cycle (by being read or written).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Boyer's recent access flags in Ohsawa's device to further reduce the number of refresh cycles required to maintain data because Boyer's device is directed to the same goal of reducing the number of refreshes required, thereby reducing power consumption and enhancing processing speed by improving bandwidth.

Regarding claims 21, 34, and 40, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claims 23, Ohsawa shows his use registers in the memory devices in Figs. 4, 5, 7, and 8.

Regarding claim 24, Ohsawa's refresh flags refer to rows as claimed.

Regarding claim 9, Ohsawa's refresh flags refer to rows. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use refresh flags for a bank since this would allow an entire bank to be shutdown if its refresh flag were not set, avoiding the need to read the refresh flag of each row.

Regarding claims 22 and 30, Ohsawa shows that his use registers are in the memory devices, however, It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the use registers to the memory controller to have more centralized control over the memory cells. Putting the use registers in the memory controller would speed up access to them.

Response to Arguments

Regarding claims 1 and 11, on page 15, fourth paragraph, and page 17, fourth paragraph, Applicant argues that "the Office Action cites Ohsawa's DRAM controller and its 'refresh flag.'" However, nowhere in the statement of rejection of claim 1 does the Office action even mention a "DRAM controller." This term is used only by Ohsawa at section 3.1, third paragraph.

The Examiner's rejection of claim 1 clearly stated that the claimed plurality of dynamically refreshable memory cells was anticipated by Ohsawa's DRAM cell array in Fig. 5 (the Examiner neglected to mention that this DRAM cell array also appears in Fig. 4).

Furthermore, the Examiner clearly stated that the dynamically changeable use registers are anticipated by Ohsawa's refresh flags in Figs. 4 and 5.

These two sets of elements (memory cells and use registers) comprise the claimed "memory device" and the Examiner specifically pointed out that both the memory cells and the use registers are anticipated by Ohsawa's Figs. 4 and 5.

What the Examiner failed to mention (because it is plainly evident) was that Ohsawa shows these memory cells and use registers together in a single "memory unit" in Fig. 4 which clearly anticipates the claimed "memory device". Ohsawa's memory unit of Fig. 4 is further detailed in Fig. 5, even though Fig. 5 is not explicitly labeled "memory unit".

Therefore, the claimed memory device is anticipated by the "memory unit" shown in Figs. 4 and 5.

It is not clear why Ohsawa mentions DRAM controller since he doesn't show it in the figures. Perhaps he intends the circuitry on the memory unit other than the DRAM cell array to be interpreted as a DRAM controller since it "controls" the DRAM cell array. Typically a DRAM controller controls the memory devices (memory units) but this interpretation doesn't seem to match Ohsawa's disclosure and figures. Since Ohsawa's disclosure is a poor translation from Japanese, perhaps the term DRAM controller was

not intended. In any case, the claimed memory device is anticipated by the shown memory unit.

Regarding claims 2 and 12, on page 16, second paragraph, and page 18, first paragraph, Applicant argues that "static mode is not 'wherein the self-refresh logic is configured to not refresh the indicated unused memory cells'". The Examiner is asserting that Ohsawa's static mode is a self-refresh mode. Furthermore, it must be noted that Ohsawa's entire disclosure is directed toward reducing the power consumed by refresh cycles and one of the main ways his device accomplishes such power reduction is by not refreshing memory cells that are not in use. He keeps track of which memory cells (or rows of memory cells, to be more accurate) are not in use with his refresh flags. He mentions in the last paragraph of section 4.3 that his simulation was done assuming the DRAM was in normal mode, but the technique of only refreshing in-use rows is just as valuable for saving power in the "static" or "standby" mode (also called self-refresh mode) when the DRAM is not being actively accessed but rather is just refreshing itself to maintain the data stored therein. Ohsawa teaches that static mode is entered "as a consequence of I/O, interruptions and so on", all of which are cases when the DRAM is not being accessed due to other activities in the system which occupy the processor. Applicant has presented no evidence whatsoever that Ohsawa's static or standby mode is different than the claimed "self-refresh" mode, therefore the rejection is maintained.

Regarding claim 10, on page 16, last paragraph, Applicant traverses the Examiner's assertion that a page of memory cells can be the same as a row of memory cells. The definition of a "page" varies from one author to the next, but certainly it was common in the art to refer to a row of memory as a page. Even given the Applicant's definition of a page ("a section of memory cells that are accessible at one time and treated as a unit of data", next to last sentence of page 16), it is clear that a page of memory cells can be a row of memory cells since a row of cells is a section of memory cells that are accessible at one time and treated as a unit of data.

Regarding claim 23, on page 19, third paragraph, Applicant argues that Ohsawa discloses a system where the use registers are "on the DRAM controller". However, as stated above, although Ohsawa mentions a DRAM controller, he shows the use flags (refresh flags) on the memory device (memory unit) itself.

Regarding claim 25, on page 20, first paragraph, Applicant argues that "Ohsawa does not describe operating the non-allocated memory at a reduced power". However, Ohsawa clearly shows operating non-allocated (not in use) DRAM memory rows at reduced power since they are not refreshed.

Regarding claim 9, Applicant argues on page 24, first paragraph, that the Examiner's rejection of claim 9 is an example of impermissible hindsight. In response, it is noted that it must be recognized that any judgment on obviousness is in a sense

necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In this case, Ohsawa clearly shows using use registers comprising bits that each correspond to a row of memory cells. It would have been obvious to one of ordinary skill in the art at the time the invention was made to similarly use registers comprising bits that each correspond to a bank of memory cells because a bank is merely a collection of rows. In other words, Ohsawa teaches using use registers corresponding to certain memory regions (rows). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use use registers corresponding to other memory regions (banks).

Conclusion

The method claims are grouped and rejected with the apparatus claims because the steps of the method are met by the disclosure of the apparatus and methods of the reference(s) as discussed above.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Primary Examiner Kevin Verbrugge by phone at (703) 308-6663.

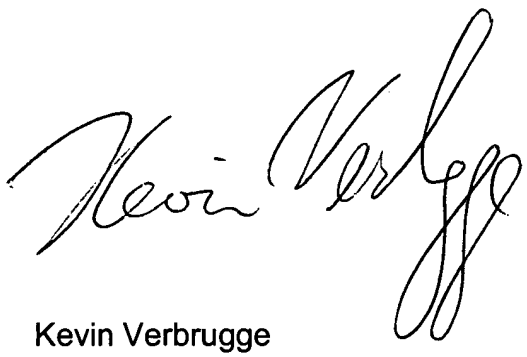
Any response to this action should be mailed to Commissioner for Patents, Washington, D.C. 20231 or faxed to

(703) 746-7238 After-final

(703) 746-7239 Official

(703) 746-7240 Non-Official/Draft

and labeled appropriately (After-final, Official, Non-Official/Draft). Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor (Receptionist).



Kevin Verbrugge
Primary Examiner
8/13/03